UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,379	01/21/2004	Sean G. Gibb	113667-025UTL	2143

27189 7590 12/12/2007

PROCOPIO, CORY, HARGREAVES & SAVITCH LLP
530 B STREET
SUITE 2100
SAN DIEGO, CA 92101

EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
12/12/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@procopio.com
PTONotifications@procopio.com

Office Action Summary	Application No.	Applicant(s)	
	10/760,379	GIBB ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 11/30/2007.

2. Claims 1-25 are pending in this application. Claims 1, 12, 15, and 21 are independent claims. This Office Action is made non-final after a RCE filed 11/30/2007.

Claim Objections

3. Claim 7 is objected to because of the following informalities:

Re claim 7, it is depending on itself.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 1, the limitation "the control signal comprising a combination of a current and a prior switching signal" is considered as new subject matter, which is not

fully disclosed, in the original specification. The original specification does not have a written description of the limitation in to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Other independent claims 12, 15, and 21 have the same rejection as cited above.

Thus, claims 2-11, 13-14, 16-20, and 22-25 are also rejected for being dependent on the rejected base claims 1, 12, 15, and 21,

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-25 cite a processor and method for performing FFT in accordance with a mathematical algorithm. However, claims 1-25 merely disclose steps/components for performing FFT without further disclosing a practical/physical application since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 1-25 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeh (U.S. 2004/0059766).

Re claim 1, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input data sequence (e.g. Figure 3 and abstract wherein the input data sequence is x(k) and paragraph [0008]), the processor comprising:

at least one FFT triplet module (e.g. Figure 3 part 37 is the triplet FFT module) having first, second and third butterfly modules connected in series (e.g. 31a, 32, and 33 modules respectively in Figure 3) by selectable multipliers for selectively performing trivial coefficient multiplication and complex coefficient multiplication on output data data sequences of adjacent butterfly modules (e.g. controlling by 36 and its complex coefficients 36b in Figure 3), wherein a selectable multiplier is selected in response to a control signal provided with each butterfly module (e.g. Figures 3 and 5-8 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), each of the at least one

FFT triplets terminating in a twiddle factor multiplier for applying a twiddle factor to an output of the third butterfly module of the respective triplet (e.g. see Figure 9 with twiddle factor multipliers as Wx), the at least one FFT triplet for receiving the input data sequence and for outputting a final output data sequence representing an FFT of the input sequence (e.g. the last stage of computation as seen in Figure 9 with BFII as the last stage of 32 input data sequence).

Re claim 2, Yeh further discloses in Figures 1-16 each butterfly module includes a radix-2 butterfly unit and a feedback memory (e.g. Figure 3 with 37 as triplet module wherein the module consists of three separate sub-modules wherein each sub-module consists of a butterfly operation and its feedback memory).

Re claim 3, Yeh further discloses in Figures 1-16 for an input data sequence of N samples, an output data sequence X(k, n) of each butterfly module is equal to $x(n)+(-1)^k x(n+N/2)$ (e.g. inverse processed in BFII of Figure 9).

Re claim 4, Yeh further discloses in Figures 1-16 at least one of the selectable multipliers for performing trivial coefficient multiplication is integrated in an adjacent butterfly module (e.g. Figure 10 with 608).

Re claim 5, Yeh further discloses in Figures 1-16 the selectable multipliers each include a multiplier and a switch for bypassing the multiplier (e.g. by the control unit in Figure 10 with Figure 14).

Re claim 6, Yeh further discloses in Figures 1-16 the first and second butterfly modules are connected by a selectable multiplier for selectively applying trivial coefficient multiplication (e.g. Figure 11B with j multiplication in BFII).

Re claim 7, Yeh further discloses in Figures 1-16 the second and third butterfly modules are connected by a selectable multiplier for performing trivial coefficient multiplication and a selectable multiplier for performing the complex coefficient multiplication W.sub.N.sup.N/8 (e.g. Figure 11B with jW and W multiplication in BFIII).

Re claim 8, Yeh further discloses in Figures 1-16 for an input data sequence having N samples, the feedback memories for the first, second and third butterfly modules hold N/2, N/4 and N/8 samples, respectively (e.g. Figure 3 with part 37 wherein each feedback memory holds appropriated size of input data).

Re claim 9, Yeh further discloses in Figures 1-16 the input data sequence is of length N, where (log.sub.2N)mod3=1, the processor having a plurality of FFT triplets in seriatim (e.g. Figure 3 wherein butterfly I, II, and III are in seriatim manner) and further including an FFT terminator having a butterfly unit (e.g. component 31a, 32, and 33 in Figure 3) and a corresponding memory sized to hold a single sample (e.g. component 2, 4, and 8 in Figure 3), the FFT terminator for receiving the output data sequence from the final twiddle factor multiplier and for performing a butterfly operation on the received output data sequence to render an FFT of the input data sequence (e.g. as the case of Figure 3).

Re claim 10, Yeh further discloses in Figures 1-16 the input data sequence is of length N, where (log.sub.2N)mod3=2, the processor having a plurality of FFT triplets in seriatim (e.g. Figure 3 wherein butterfly I, II, and III are in seriatim manner) and further including an FFT terminator having first and second butterfly units having corresponding memories sized to hold two samples and a single sample respectively (e.g. Figure 3), the

first butterfly unit connected to the second butterfly unit by a selectable multiplier for selectively multiplying the output of the first butterfly unit by –j (e.g. Figures 4-6), the FFT terminator for receiving the output data sequence from the final twiddle factor multiplier and for performing a pair of butterfly operations on the received output data sequence to render an FFT of the input data sequence (e.g. as the case of Figure 10 and its corresponding Figure 11A).

Re claim 11, Yeh further discloses in Figures 1-16 the twiddle factor multiplier is a cordic rotator (e.g. component 208 in Figure 5).

Re claim 12, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of N samples (e.g. abstract and Figure 3 wherein the input is either x(n)/X(N) depending on the processed of FFT/IFFT respectively), the processor comprising:

at least one FFT triplet module (e.g. part 37 in Figure 3), the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output data sequence in accordance with a butterfly operation performed on the input data sequence (e.g. 31a and 8 in Figure 3), the first stage radix-2 butterfly unit having a first feedback memory connected thereto;

a second FFT stage having a selectable multiplier for selectively multiplying the first stage output data sequence by a trivial coefficient, wherein a selectable multiplier is selected in response to a first control signal provided with the second FFT stage module (e.g. Figures 3 and 5 wherein the base butterfly operation is seen in Figure 4 with add and

subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), and a second stage radix-2 butterfly unit for providing a second stage output data sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto (e.g. part 32 and 4 in Figure 3); and

a third FFT stage having a multiply selectable multiplier for selectively multiplying the second stage output data sequence by at least one of the trivial coefficient and a complex coefficient, wherein a selectable multiplier is selected in response to a second control signal provided with the third FFT stage module (e.g. Figures 3 and 6 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the multiply selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence (e.g. part 33 and 2 in Figure 3) (e.g. wherein each of the stage of BF is clearly addressed or shown in Figures 4-6 respectively).

Re claim 13, Yeh further discloses in Figures 1-16 each of the first, second and third stage output data sequences X(k,n) is equal to $x(n)+(-1)^k x(n+N/2)$ (e.g. inverse processed in BFII of Figure 9).

Re claim 14, Yeh further discloses in Figures 1-16 at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial coefficient multiplication to a received input data sequence (e.g. Figure 9 with BFII and BFIII).

Re claim 15, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of N samples (e.g. triplet 37 in Figure 3 and the abstract wherein the input data sequence is either x(n)/X(N) depending on the processed FFT/IFFT respectively), the processor comprising:

at least one FFT triplet module (e.g. triplet 37 in Figure 3), the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output data sequence in accordance with a butterfly operation performed on the input data sequence, the first stage radix-2 butterfly unit having a first feedback memory connected thereto (e.g. BFI 31a and 8 in Figure 3);

a second FFT stage having a multiply selectable multiplier for selectively multiplying the first stage output data sequence by at least one of the trivial coefficient, wherein a selectable multiplier is selected in response to a first control signal provided with the second FFT stage module (e.g. Figures 3 and 5 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal

comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), and a constant complex coefficient, and a second stage radix-2 butterfly unit for providing a second stage output data sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto (e.g. BFII 32 and 4 in Figure 3); and

a third FFT stage having a selectable multiplier for selectively multiplying the second stage output data sequence by a trivial coefficient, wherein a selectable multiplier is selected in response to a second control signal provided with the third FFT stage module (e.g. Figures 3 and 6 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence (e.g. part 33 and 2 in Figure 3) (e.g. wherein each of the stage of BF is clearly addressed or shown in Figures 4-6 respectively).

Re claim 16, Yeh further discloses in Figures 1-16 each of the first, second and third stage output data sequences X(k,n) is equal to $x(n)+(-1)^k x(n+N/2)$ (e.g. inverse processed in BFII of Figure 9).

Re claim 17, Yeh further discloses in Figures 1-16 at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial coefficient multiplication to a received input data sequence (e.g. Figure 9 with BFII and BFIII).

Re claim 18, Yeh further discloses in Figures 1-16 an FFT terminator determined in accordance with the length N of the input data sequence (e.g. either Figure 3 or Figure 10).

Re claim 19, Yeh further discloses in Figures 1-16 the FFT terminator includes a butterfly module having a memory sized to store a single sample, for receiving as a terminator input, the output of the third FFT stage multiplier and for performing a butterfly operation on the terminator input to render an FFT of the input data sequence of N samples (e.g. as with the BFI as seen in Figure 3).

Re claim 20, Yeh further discloses in Figures 1-16 the FFT terminator includes a first butterfly module having a memory sized to store a pair of samples, for receiving as a terminator input, the output of the third stage multiplier and for performing a butterfly operation on the terminator input (e.g. Figures 4-6), and a second butterfly module connected to the first butterfly module of the terminator by a selectable multiplier, the selectable multiplier for selectively multiplying the output of the first butterfly module of the terminator by -j, the second butterfly module having a memory sized to store a single sample and for performing a butterfly operation on the selectively multiplied output of the first butterfly module of the terminator to render an FFT of the output data sequence (e.g. as with the BFI and BFII as seen in Figure 10 and its corresponding Figure 11A).

Re claim 21, Yeh discloses in Figures 1-16 Yeh discloses in Figures 1-16 a method of performing an FFT on a data sequence of N samples in an FFT processor having a butterfly module (e.g. Figure 3 and abstract), the method (e.g. for purposes of illustration Figures 2-3 are used to illustrate the features of prior art) comprising: for all integers x according to 1.ltoreq.x.ltoreq.log.sub.2N (e.g. there are 16 input data label as X[0] to X[15]), repeating the steps of receiving and buffering $N/2^x$ samples at a time from a data sequence having N samples (e.g. sampling and initialization), generating a 2-point FFT using the n.sup.th and the 24 (n + N 2 x) the samples (e.g. X[0] and X[8] are computed together); selectively multiplying the generated 2-point FFT data sequence by a complex valued multiplicand (e.g. as seen in Figure 2 only the last four data are multiplied with j); wherein a multiplier is selected in response to a control signal provided with each butterfly module (e.g. Figures 3 and 5-8 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10); terminating the FFT using a termination data sequence determined in accordance with a (log.sub.2N)mod3 relationship to obtain an FFT of the sequence of N samples; and outputting the FFT of the sequence of N samples (e.g. Figure 3 or Figure 10).

Re claim 22, Yeh further discloses in Figures 1-16 the complex valued multiplicand is selected from a list including 1, - j , sqrt(2)/2 - jsqrt(2)/2 ,and a complex twiddle factor coefficient (e.g. Figures 3-6).

Re claim 23, Yeh further discloses in Figures 1-16 (log.sub.2N)mod3=1 and the step of terminating the FFT includes buffering a sample received from the final selective multiplication and performing a 2-point FFT using the buffered sample and the subsequent sample in the data sequence to obtain the FFT of the data sequence of N samples (e.g. as with the BFI as seen in Figure 3).

Re claim 24, Yeh further discloses in Figures 1-16 (log.sub.2N)mod3=2 and the step of terminating the FFT (e.g. Figures 4-6) includes: buffering a pair of samples received from the final selective multiplication and performing pair-wise 2-point FFTs using the two buffered samples and the two subsequent samples in the data sequence; selectively multiplying the result of the pair-wise 2 point FFT by –j (e.g. Figures 4-6 as butterfly component for BFI, BFII, and BFIII); and buffering a sample received from the selective multiplication of the pair-wise 2-point FFT and performing a 2-point FFT using the buffered sample and the subsequent sample in the data sequence to obtain the FFT of the data sequence of N samples (e.g. as with the BFI and BFII as seen in Figure 10 and its corresponding Figure 11A).

Re claim 25, Yeh further discloses in Figures 1-16 an FFT terminator determined in accordance with the length N of the input data sequence (e.g. either Figure 3 or Figure 10).

Response to Amendment

The amendment filed 11/30/2007 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall

introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

The newly added limitations to each of independent claims 1, 12, 15, and 21 as "the control signal comprising a combination of a current and a prior switching signal" is considered as new matter introduce into the original specification since the original specification does not clearly and explicitly point-out the limitation the control signal comprising a combination of a current and a prior switching signal.

Applicant is required to cancel or explicitly point-out within the original specification the support of the new matter in the reply to this Office Action.

Response to Arguments

9. Applicant's arguments filed 11/30/2007 have been fully considered but they are not persuasive.

a. The applicant argues in pages 10-11 for claims 1-25 rejected under 35 U.S.C. 101 that the claims are statutory since they describe a FFT processor and further each of claim clearly discloses the FFT processor comprising multiple modules with a control signal wherein the control signal comprising a combination of a current and a prior switching signal.

The examiner respectfully submits that all the claims merely disclose FFT operations on generic corresponding hardware components. The claims do not disclose any practical application as necessary. Further, the claims with just mathematical operations as FFT operations would preempt all existing practical

application of utilizing the FFT operations. The processor comprising control signals for controlling the FFT operations is just generic hardware component for implementing the FFT operations.

b. The applicant argues in page 12 for all claims that the newly added limitations into each independent claims are not disclosed by the cited reference by Yeh, particularly the selectable multiplier is selected in response to a control signal provided with each butterfly module, and the control signal comprises a combination of a current and a prior switching signal as cited in the claimed invention.

The examiner respectfully submits that the newly added limitations are clearly addressed in the above rejection. To reiterate, the cited reference by Yeh clearly and expressively discloses the limitations in Figures 3-8 wherein the selectable multiplier function is placed within the BFII and BFIII modules corresponding to Figures 5-6 for multiplying complex j factor as seen in component 208 Figure 5 and components 308 and 309 in Figure 6. These individual separated control signals come directly from the control unit as seen in Figure 3. Further, the control signal comprises a combination of a current and a prior switching signal as for switching to multiplying the complex j or to bypass through the controlled multiplexer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

December 6, 2007